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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/653,785	09/02/2003	Edward T. Grochowski	42P4898XC	6927

8791 7590 10/24/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
MCCARTHY, CHRISTOPHER S	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 10/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/653,785	GROCHOWSKI ET AL.	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-11,13-17,19-22 and 25-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25-29* is/are allowed.

6)☒ Claim(s) *1-3,6-11,13-17,19-22 and 30-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *response to arguments*.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 7, 8, 15, 20, 21, 30-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Kogge et al U.S. Patent 4,912,707.

As per claim 1, Kogge teaches a processor comprising: a protected execution unit including a first execution unit and a second execution unit, the fist execution unit and the second execution unit to process instructions in lock step (column 5, lines 45-48; column 7, lines 47-51); a check unit coupled to the first execution unit and the second execution unit, the check unit to detect an error associated with processed instructions (column 2, lines 47-50, wherein there is respective check unit coupled to each execution unit performing the same function); and at least one replay queue coupled to the check unit and to the protected execution unit, the at least one replay queue to issue a plurality of instructions to the protected execution unit for processing, to track the plurality of issued instructions issued to the protected execution unit, and to selectively reissue one or more of the plurality of instructions to the protected execution unit when the check unit detects an error (column 2, lines 47-58; column 3, lines 36-38, column 5, lines 64-68; column 6, line 54 – column 7, line 13; wherein, the instruction memory (20)

includes a address register which issues instructions to the ALU and upon a failure, as indicated/selected, to the memory module inclusive of the address register, by the checkpoint retry address, reissues the indicated instruction(s)).

As per claim 7, Kogge teaches the processor of claim 1, wherein the processor implements a recovery algorithm if an instruction that triggers a replay generates a mismatch when it is replayed (column 9, lines 29-30, 35-37).

As per claim 8, Kogge teaches a method for executing instructions with high reliability (column 5, lines 45-48), comprising: temporarily storing a plurality instructions in replay buffer (column 2, lines 54-58; column 3, lines 36-38); issuing a plurality of instructions stored in the replay buffer to a first execution unit and a second execution unit (column 5, lines 45-48; column 7, lines 47-51); receiving a plurality of results from the first execution unit and the second execution unit in response to the plurality of the instructions issued from the replay buffer (column 5, lines 42-58); checking the plurality of results generated by the first execution unit and the second execution unit in response to the plurality of the instructions issued from the replay buffer (column 5, lines 48-52; column 6, line 59 – column 7, line 13); signaling the replay buffer to reissue one or more instructions of the plurality of instructions issued to the first execution unit and the second execution unit of the protected execution unit, if an error is detected during the checking (column 6, line 59 – column 7, line 13).

As per claim 15, Kogge teaches a computer system comprising: a processor that includes: a protected execution unit to execute instructions in a manner that facilitates soft error detection (column 7, lines 30-33); a check unit to monitor the protected execution unit and to generate a signal when an error is indicated (column 6, lines 59-63); a replay unit coupled to the protected

execution unit and the check unit, the replay unit to temporarily store a plurality of instructions and provide the plurality of instructions to the protected execution unit for execution, the replay unit to track the plurality of instructions until they are retired, and the replay unit to repetitively replay selected instructions of the plurality of instructions when the check unit indicates an error (column 2, lines 47-58; column 3, lines 36-38, column 5, lines 64-68; column 6, line 54 – column 7, line 13); and a storage structure coupled to the processor, the storage structure to store a recovery algorithm, the storage structure to provide the recovery algorithm to the processor when a specified number of replays of the selected instructions does not eliminate the mismatch (column 2, lines 47-58; column 3, lines 36-38, column 5, lines 64-68; column 6, line 54 – column 7, line 30; wherein, the selected/indicated instructions are replayed twice and upon a second failure, are made available to for analysis, wherein a software branch, as taught by Kogge, for an analysis routine must be stored on a storage structure coupled to the processor).

As per claim 20, Kogge teaches the computer system of claim 15, wherein the protected execution unit comprises first and second execution units and the replay unit provides identical instructions to the first and second execution units (column 5, lines 45-48; column 2, lines 54-58).

As per claim 21, Kogge teaches a processor comprising: first and second execution cores to process identical instructions in lock step (column 7, lines 47-51), each execution core having a fetch stage, a decode stage, a register stage, an execute stage, a detect stage, and a retirement stage in an instruction execution pipeline (figure 1, wherein, the fetch stage is the fetching of instructions in the memory for execution, the decode stage is the instruction decoder (28), the register stage is the address register (38), the execute stage is the ALU (22), the detect stage is

the error checker (74) or comparator (69), the retirement stage can be either executable instructions that do not cause an error and are retired as processed, or can be interpreted as the instructions that cause the same error twice and are flagged for analysis), the decode stage of each execution core including a replay unit to track a plurality of instructions that have yet to retire in the retirement stage (column 6, line 54 – column 7, line 30, wherein, the instruction decoder is an intermediary between the instruction memory and the ALU and, therefore, integral in the reissuing of indicated instructions); and a check unit coupled to the first and second execution cores and the replay unit, the check unit to compare instruction results generated by the execution cores in their respective detect stages prior to retirement and to trigger the replay unit to resteer the first and second execution cores to re-execute one or more selected instructions in their respective instruction execution pipelines when the instruction results generate a mismatch (column 6, line 51 – column 7, line 30).

As per claim 30, Kogge teaches a check unit comprising: a plurality of comparators, one comparator for each corresponding pair of execution units in a first execution core and a second execution core to compare execution results (column ; an OR gate having inputs coupled to the outputs of the plurality of comparators, the OR gate to generate a logic value one at its output when any one of the plurality of comparators indicate that their corresponding execution results do not match; and wherein the output of the OR gate indicates an error when the check unit is enabled (column 8, lines 55-67).

As per claim 31, Kogge teaches the check unit of claim 30, further comprising: an AND gate having a first input coupled to an enable signal and a second input coupled to the output of

the OR gate, the AND gate to enable the OR gate to generate an error signal and indicate an error in response to the enable signal (column 7, lines 7-12).

As per claim 32, Kogge teaches the check unit of claim 30, further comprising: a counter having an input coupled to the output of the OR gate, the counter to track a number of replays triggered by an instruction (column 7, lines 3-30, wherein, a first and second latch are set upon a respective first and second error; thus a ripple count effect occurs since upon a first error, latch one sets, and upon a second error, latch two sets).

As per claim 33, Kogge teaches the check unit of claim 32, wherein if the number of replays triggered by an instruction is equal to a specified number, the counter to invoke a recovery routine (column 7, lines 3-30, wherein a recovery/analysis routine is started upon the same error occurring twice to set both latches).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kogge in view of Bauer et al. U.S. Patent 5,604,753.

As per claim 2, Kogge teaches the processor of claim 1. Kogge does not explicitly teach wherein the instructions are flushed from the execution unit when the check unit indicates an

error. Bauer does teach wherein the instructions are flushed from the execution unit when the check unit indicates an error (column 9, lines 33-42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the flushing process of Bauer in the processor of Kogge. It would have been obvious to one of ordinary skill to use the flushing process of Bauer in the processor of Kogge because Bauer teaches the importance of flushing the pipeline to prevent an error from permanently changing the state of the computer and allows for full, functional resources; an explicit desire of Kogge (column 9, line 48 – column 10, line 9).

5. Claims 3, 9-11, 13, 14, 16, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kogge in view of Shen et al. U.S. Patent 5,659,721.

As per claim 3, Kogge teaches the processor of claim 1 and a replay queue (column 2, lines 47-58). Kogge does not teach wherein the replay queue includes first and second pointers to indicate a next instruction to issue and a next instruction to retire. Shen does teach wherein the replay queue includes first and second pointers to indicate a next instruction to issue and a next instruction to retire (column 22, line 25-33; column 21, lines 55-63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the pointer system of Shen in the replay queue of Kogge. One of ordinary skill in the art would have been motivated to use the pointer system of Shen in the replay queue of Kogge because the point of the pointer is keep track of the instruction at hand as well as other instructions, such as the next instruction to be processed, this sequential instruction structure is an explicit instruction address format taught by Kogge (column 3, lines 57-63).

As per claims 9, 10, and 11, Kogge teaches the method claim 8, wherein issuing the instruction comprises staging the instruction to the protected execution unit (column 5, 45-48). Kogge does not explicitly teach the adjusting a first flag in the buffer to indicate the instruction has been issued which comprises setting a first pointer to indicate a buffer slot in which the issued instruction is stored, and setting a second pointer to indicate a buffer slot in which a next instruction to retire is stored. Shen does teach the adjusting a first flag in the buffer to indicate the instruction has been issued which comprises setting a first pointer to indicate a buffer slot in which the issued instruction is stored, and setting a second pointer to indicate a buffer slot in which a next instruction to retire is stored (column 21, line 47 – column 22, line 6, wherein a flag is inherent in a pointer as just a marker for some characteristic thereof). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the pointer system of Shen in the method of Kogge. One of ordinary skill in the art would have been motivated to use the pointer system of Shen in the replay queue of Kogge because the point of the pointer is keep track of the instruction at hand as well as other instructions, such as the next instruction to be processed, this instruction is an explicit instruction address format taught by Kogge (column 3, lines 57-63).

As per claim 13, Kogge teaches the method of claim 8. Kogge does not explicitly teach retiring the instruction when no error is indicated. Shen does teach retiring the instruction when no error is indicated (column 34, lines 10-19). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the retire instruction process of Shen in the method of Kogge. One of ordinary skill in the art would have been motivated to use the retire instruction process of Shen in the method of Kogge because Shen teaches the retiring of

the instruction as to allow the system to reclaim resources needed for subsequent instructions; an explicit desire of Kogge (column 9, lines 26-28, 47-50).

As per claim 14, Kogge teaches the updating an architectural state data with the result generated by the instruction (column 9, lines 26-28). However, Kogge does not explicitly teach wherein retiring the instruction comprises: adjusting a second pointer to indicate the instruction has retired. Shen does teach wherein retiring the instruction comprises: adjusting a second pointer to indicate the instruction has retired (column 34, lines 32-41). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the pointer system of Shen in the method of Kogge. One of ordinary skill in the art would have been motivated to use the pointer system of Shen in the replay queue of Kogge because the point of the pointer is keep track of the instruction at hand as well as other instructions, such as the next instruction to be processed, this instruction is an explicit instruction address format taught by Kogge (column 3, lines 57-63).

As per claim 16, Kogge teaches the computer system of claim 15 and a replay unit. Kogge does not explicitly teach wherein the replay unit includes first and second pointers to indicate a next instruction to issue and a next instruction to retire, respectively. Shen does teach wherein the replay unit includes first and second pointers to indicate a next instruction to issue and a next instruction to retire, respectively (column 22, lines 25-33; column 34, lines 32-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the pointer system of Shen in the method of Kogge. One of ordinary skill in the art would have been motivated to use the pointer system of Shen in the replay queue of Kogge because the point of the pointer is keep track of the instruction at hand as well as other instructions, such as

the next instruction to be processed, this instruction is an explicit instruction address format taught by Kogge (column 3, lines 57-63). Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the retire instruction process of Shen in the method of Kogge. One of ordinary skill in the art would have been motivated to use the retire instruction process of Shen in the method of Kogge because Shen teaches the retiring of the instruction as to allow the system to reclaim resources needed for subsequent instructions; an explicit desire of Kogge (column 9, lines 26-28, 47-50).

As per claim 22, Kogge teaches the processor of claim 21 and a replay unit wherein each replay unit includes buffer slots to store instructions for execution (column 4, lines 13-44). Kogge does not explicitly teach the first and second pointers to indicate a next instruction to issue and a next instruction to retire, respectively. Shen does teach the first and second pointers to indicate a next instruction to issue and a next instruction to retire, respectively (column 22, lines 25-33; column 34, lines 32-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the pointer system of Shen in the method of Kogge. One of ordinary skill in the art would have been motivated to use the pointer system of Shen in the replay queue of Kogge because the point of the pointer is keep track of the instruction at hand as well as other instructions, such as the next instruction to be processed, this instruction is an explicit instruction address format taught by Kogge (column 3, lines 57-63). Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the retire instruction process of Shen in the method of Kogge. One of ordinary skill in the art would have been motivated to use the retire instruction process of Shen in the method of Kogge because

Shen teaches the retiring of the instruction as to allow the system to reclaim resources needed for subsequent instructions; an explicit desire of Kogge (column 9, lines 26-28, 47-50).

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kogge in view Grohoski U.S. Patent 5,247,628.

As per claim 6, Kogge teaches the processor of claim 1, wherein the execution units operate in lock step when the processor is in a high reliability mode (column 5, lines 45-48). Kogge does not explicitly teach wherein the execution units independently when the processor is in a high performance mode. Grohoski does teach wherein the execution units operate in lock step when the processor is in a high reliability mode and the execution units independently when the processor is in a high performance mode (column 1, lines 55-64). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the execution unit process of Grohoski to the process of Kogge. One of ordinary skill in the art would have been motivated to combine the execution unit process of Grohoski to the process of Kogge because Grohoski teaches the advantage of processing normally in high performance mode, but being able to switch to high reliability mode of redundant processing upon the occurrence of an error event; this is an explicit desire of Kogge (column 5, lines 45-52).

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kogge in view of Shen as applied to claim 16, and in further view of Bauer.

As per claim 17, Kogge in view of Shen teaches the computer system of claim 16. Kogge in view of Shen does not teach wherein the execution units are flushed prior to the replay

when an error is indicated. Bauer does teach wherein the execution units are flushed prior to the replay when an error is indicated (column 9, lines 33-42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the flushing process of Bauer in the processor of Kogge. It would have been obvious to one of ordinary skill to use the flushing process of Bauer in the processor of Kogge because Bauer teaches the importance of flushing the pipeline to prevent an error from permanently changing the state of the computer; an explicit desire of Kogge (column 9, line 50 – column 10, line 9).

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kogge in view of Shen as applied to claim 16, and in further view of Hennessy.

As per claim 19, Kogge in view of Shen teaches the computer system of claim 16. Kogge in view of Shen does not explicitly teach wherein the storage structure is a non-volatile memory structure. Hennessey does teach wherein the storage structure is a non-volatile memory structure (page G-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the non-volatile memory in the structure of Kogge. One of ordinary skill in the art would have been motivated to use the non-volatile memory in the structure of Kogge because Hennessey teaches wherein the non-volatile memory is integral in a format wherein a program should be retained when the power is switched off. Kogge teaches wherein a software-controlled recovery program is needed to activate his recovery process (column 9, lines 40-42). It would be an implicit desire of Kogge to retain the software recovery program in the system in the event of a power loss so as to not having to re-program the entire process upon a power loss.

Allowable Subject Matter

9. Claims 25-29 are allowed.

Reasons for Allowance

10. The following is an examiner's statement of reasons for allowance: When read as a whole claims 25 and 28 are allowable with respect to the following limitations:

With respect to claim 25, Kogge does not teach the combination of a first parity protected storage structure having a first parity bit and a second parity-protected storage structure having a second parity bit and in combination the proceeding claimed limitations; nor does the examiner find reason for Kogge to have desire to combine such a feature

With respect to claim 28, Kogge does not teach a first protected storage structure having a first plurality of error correction control bits; a second protected storage structure having a second plurality of error correction control bits and in combination the proceeding claimed limitations; nor does the examiner find reason for Kogge to have desire to combine such a feature

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

11. Applicant's arguments filed 7/24/06 have been fully considered but they are not persuasive.

With respect to applicant's arguments, the applicant argues that checkpoint address register of Kogge does not teach the replay unit/queue/buffer. The examiner wishes to clarify that the checkpoint address register merely indicates the instruction address register as to which instruction was found to be in error. The instruction address register is taught to be inclusive in the actual instruction memory of Kogge (column 3,, lines 36-38); therefore, the instruction memory with all its inclusive components (address register) is interpreted as the replay unit/buffer/queue as the instructions are stored there and processed sequentially therefrom.

The applicant also argues that the check unit of Kogge is not coupled to the replay queue/buffer/unit (instruction memory). Looking at figure 1, the check unit is coupled by line 67 to the OR comparator 69 then is coupled by line 92 to the address register 30 which is coupled/inclusive to the instruction memory; so the broadly interpreted the check unit is coupled to the replay queue/buffer/unit.

The applicant also argues that the address registers of Kogge merely store addresses and not instructions. The examiner reiterates the above argument that the instruction address register is inclusive to the instruction memory, which does store instructions, and the module as a whole teaches the needed the limitations.

In light of the above arguments, all applicable rejected claims stand.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: See attached PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christopher S. McCarthy
Examiner
Art Unit 2113